Claims:

1. A method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, comprising the steps of:

forming a bottom electrode of the charge storage capacitor and a bottom electrode of the data storage capacitor on an integrated circuit substrate;

forming a ferroelectric layer on the bottom electrode of the data storage capacitor;

forming a top electrode layer on the ferroelectric layer;

forming a first encapsulation layer on the bottom electrode of the charge storage capacitor and a second encapsulation layer on the bottom electrode of the data storage capacitor including the ferroelectric layer and the top electrode, wherein the first encapsulation layer and the second encapsulation are formed simultaneously; and

forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer,

wherein the first encapsulation layer is a dielectric layer of the charge storage capacitor.

2. The method for forming an integrated circuit according to claim 1, wherein the first and second encapsulation layers comprise PZT.

3. The method for forming an integrated circuit according to claim 2, wherein the first and second encapsulation layers are formed at a temperature as high as 700 °C.

4. The method for forming an integrated circuit according to claim 2, wherein the first and second encapsulation layers are formed with plasma damage to improve linear dielectric performance.

5. The method for forming an integrated circuit according to claim 1, wherein the first and second encapsulation layers include Pb-based perovskite dielectrics, aluminum oxide, tantalum oxide, $BaTiO_3$, or other dielectrics.

6. The method for forming an integrated circuit according to claim 1, further comprising the steps of:

etching the first interlayer dielectric layer to form a first opening to expose the first encapsulation layer;

etching the second interlayer dielectric layer and the second encapsulation layer to form a second opening to expose the top electrode of the data storage capacitor; and

forming a first local interconnect electrode in the first opening and a second local interconnect electrode in the second opening.

7. The method for forming an integrated circuit according to claim 2, wherein the first local interconnect electrode comprises part of the charge storage capacitor.

8. A method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, comprising the steps of:

forming a bottom electrode of the charge storage capacitor and a bottom electrode of the data storage capacitor on an integrated circuit substrate;

forming a first ferroelectric layer on the bottom electrode of the charge storage capacitor and a second ferroelectric layer on the bottom electrode of the data storage capacitor;

forming a first top electrode on the first ferroelectric layer and a second top electrode on the second ferroelectric layer;

forming a first encapsulation layer on the bottom electrode of the charge storage capacitor, including the first ferroelectric layer and the first top layer;

forming a second encapsulation layer on the bottom electrode of the data storage capacitor, including the second ferroelectric layer and the second top layer, wherein the first encapsulation layer and the second encapsulation are formed simultaneously;

forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer,

etching the first interlayer dielectric layer to form a first opening to expose the first encapsulation layer;

etching the second interlayer dielectric layer and the second encapsulation layer to form a second opening to expose the top electrode of the data storage capacitor; and

forming a first local interconnect electrode in the first opening and a second local interconnect electrode in the second opening,

wherein the first local interconnect electrode comprises part of the charge storage capacitor.

9. The method for forming an integrated circuit according to claim 8, wherein the first and second encapsulation layers comprise PZT.

10. The method for forming an integrated circuit according to claim 9, wherein the first and second encapsulation layers are formed at a temperature as high as 700 °C.

11. The method for forming an integrated circuit according to claim 9, wherein the first and second encapsulation layers are formed with plasma damage to improve linear dielectric performance.

12. The method for forming an integrated circuit according to claim 8, wherein the first and second encapsulation layers include Pb-based perovskite dielectrics, aluminum oxide, tantalum oxide, $BaTiO_3$, or other dielectrics.

13. The method for forming an integrated circuit according to claim 8, wherein the bottom electrode is electrically isolated.

14. The method for forming an integrated circuit according to claim 8, wherein the top electrode is electrically isolated.

15. The method for forming an integrated circuit according to claim 8, wherein the bottom electrode forms a first electrode of the charge storage capacitor, the first ferroelectric layer and the first encapsulation layer form a

dielectric layer of the charge storage capacitor, and the first local interconnect electrode forms a second electrode of the charge storage capacitor.

16. The method for forming an integrated circuit according to claim 8, wherein the first top electrode forms a first electrode of the charge storage capacitor, the first encapsulation layer forms a dielectric layer of the charge storage capacitor, and the first local interconnect electrode forms a second electrode of the charge storage capacitor.

17. A method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, comprising the steps of:

forming a bottom electrode of the charge storage capacitor and a bottom electrode of the data storage capacitor on an integrated circuit substrate;

forming a first ferroelectric layer on the bottom electrode of the charge storage capacitor and a second ferroelectric layer on the bottom electrode of the data storage capacitor;

forming a top electrode layer on the first and second ferroelectric layers;

etching the top electrode layer to remove from the first ferroelectric layer and to form a top electrode of the data storage capacitor on the second ferroelectric layer;

forming a first encapsulation layer on the bottom electrode of the charge storage capacitor including the first encapsulation layer and a second encapsulation layer on the bottom electrode of the data storage capacitor including the second ferroelectric layer and the top electrode; and

forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer,

wherein the first encapsulation layer and the second encapsulation are formed simultaneously.

18. The method for forming an integrated circuit according to claim 17, wherein the first and second encapsulation layers comprise PZT.

19. The method for forming an integrated circuit according to claim 17, wherein the first and second encapsulation layers include Pb-based perovskite dielectrics, aluminum oxide, tantalum oxide, $BaTiO_3$, or other dielectrics.

20. The method for forming an integrated circuit according to claim 17, further comprising the steps of:

etching the first interlayer dielectric layer to form a first opening to expose the first encapsulation layer;

etching the second interlayer dielectric layer and the second encapsulation layer to form a second opening to expose the top electrode of the data storage capacitor; and

forming a first local interconnect electrode in the first opening and a second local interconnect electrode in the second opening.

21. The method for forming an integrated circuit according to claim 20, wherein the first local interconnect electrode comprises part of the charge storage capacitor.

22. The method for forming an integrated circuit according to claim 17, wherein the first ferroelectric layer and the first encapsulation layer form a dielectric layer of the charge storage capacitor.